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PATENT

Case Docket No. SIMTECH.088RAC
Date: February 28, 2000
Page 1

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

Sir:

Transmitted herewith for filing is the continuation application of reissue application of

Inventor: **Mark Moshayedi**
For: **APPARATUS FOR STACKING SEMICONDUCTOR CHIPS**

Enclosed are:

(X) A single-column copy of the specification, claims, and abstract.

(X) Informal/formal duplicates of the printed drawings of the issued patent.

(X) Preliminary Amendment in 4 pages.

(X) Copy of Reissue Application Declaration.

(X) Copy of Supplemental Reissue Application Declaration.

(X) Second Supplemental Reissue Application Declaration.

(X) Copy of Power of Attorney by Assignee.

(X) Copy of small entity declaration from prior application.

(X) Copy of Offer to Surrender and Assent of Assignee to Reissue.

(X) Reissue Application Fee Determination Record.

(X) Return prepaid postcard.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment to Account No. 11-1410. A duplicate copy of this sheet is enclosed.

(X) A check in the amount of $345 to cover the filing fee is enclosed.

John R. King
Registration No. 34,362
Attorney of Record

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COPY

Applicant or Patentee: Mark Moshayedi
Serial or Patent No. : Unknown
For: METHOD AND APPARATUS FOR STACKING SEMICONDUCTOR CHIPS

Attorney's Docket No.: SIMTECH.019A
Filed or Issued: Herewith

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) AND 1.27(c) - SMALL BUSINESS CONCERN)

COPY

I hereby declare that I am

[] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: Simple Technology Incorporated
ADDRESS OF CONCERN 3001 Daimler Street, Santa Ana, California 92705

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled METHOD AND APPARATUS FOR STACKING SEMICONDUCTOR CHIPS by inventor Mark Moshayedi described in

[X] the specification filed herewith
[] application serial no. , filed
[] patent no. , issued

I have not assigned, granted, conveyed or licensed, and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights in the invention must file separate verified statements averring to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor if that person had made the invention under 37 CFR 1.9(c) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

*NOTE:
Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27).

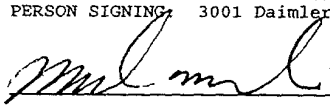
FULL NAME:
ADDRESS:
[] INDIVIDUAL [] SMALL BUSINESS CONCERN [] NONPROFIT ORGANIZATION

FULL NAME:
ADDRESS:
[] INDIVIDUAL [] SMALL BUSINESS CONCERN [] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: Mark Moshayedi
TITLE OF PERSON OTHER THAN OWNER: President
ADDRESS OF PERSON SIGNING: 3001 Daimler Street, Santa Ana, CA 92705

SIGNATURE  DATE: 3/20/95

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Docket No.: **SIMTECH.088RAC**
Date: February 28, 2000

REISSUE APPLICATION FEE DETERMINATION RECORD

CLAIMS AS FILED - PART I

	CLAIMS IN PATENT	NUMBER FILED IN REISSUE APPLICATION	NUMBER EXTRA	RATE	FEE
BASIC FEE					$345
TOTAL CLAIMS	15	6	0	$9	$0
INDEP. CLAIMS	2	1	0	$39	$0
		TOTAL FILING FEE			$0

(X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-1410. A duplicate copy of this sheet is enclosed.

(X) A check in the amount of $345 to cover the filing fee is enclosed.

(X) Return prepaid postcard.

John R. King
Registration No. 34,362
Attorney of Record

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SIMTECH.088RAC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Mark Moshayedi	) Group Art Unit: Unknown
Appl. No.	:	Unknown	)
Filed	:	Herewith	)
For	:	APPARATUS FOR STACKING SEMICONDUCTOR CHIPS	)
Examiner	:	Unknown	)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicant respectfully requests that the following amendments be entered before examination of the above-identified continuation application.

IN THE SPECIFICATION:

Please amend the specification by inserting the following before "Background Of The Invention":

This application is a continuation of co-pending application Serial No. 09/064,348, filed April 22, 1998, which is a reissue application of U.S. Patent No. 5,514,907, issued May 7, 1996, now surrendered.

IN THE CLAIMS:

Please cancel Claims 1-34 without prejudice or disclaimer.

Please add the following new claims:

35. (New) A multi-chip memory module comprising:

at least two identical, standard surface mount memory chips, each chip having identical pins arranged in respective pin positions along a side of the chip, the pin positions of the chips being identical, a first pin position being at one end of the chip and a last pin position being at the other end of the chip with intermediate pin positions therebetween, the chips being stacked with an upper one of the chips positioned above a lower one of the chips, the upper and lower chips further being arranged with corresponding pin positions above each other generally in vertical alignment;

first and second support structures, each support structure having a generally uniform rectangular cross-sectional shape and also having upper and lower series of contacts electrically connected to said two identical chips, respectively, through at least some of said pins, each series of contacts having contacts corresponding to the first and last pin positions along the side of the chip, at least some of said contacts in the upper and lower series corresponding to intermediate pin positions of said pins; and

a conductive path electrically connecting a first contact in the lower series of contacts with a second contact in the upper series of contacts, the first contact corresponding to a pin position of a pin of the lower-most chip that is unused in the memory module, and the second contact corresponding to a functional pin with a different pin position than that of the unused pin so as to provide electrical access to the functional pin from the pin position corresponding to the first contact.

36. (New) A module as in Claim 35, wherein the conductive path electrically connects only two of the contacts.

37. (New) A module as in Claim 35, wherein each support structure is comprised of a printed circuit board material on which the upper and lower series of contacts are disposed, and the pins of the lower chip are disposed relative to a bottom surface of the support structure such that when the multi-chip module is surface mounted to the memory board at least some of the pins of the lower chip are soldered to the lower series of contacts on the support structure and to the memory board.

38. (New) A module as in Claim 35, wherein the conductive path extends upward from the first contact to a first point above a level of the upper series of contacts, over to a second point generally above the second contact, and down to the second contact.

39. (New) A module as in Claim 35, wherein at least a portion of the conductive path is supported by one of the first and second support structures.

40. (New) A module as in Claim 35, wherein the conductive path comprises a conductive trace and at least one solder filled via.

COMMENTS

This application is a continuation of co-pending application Serial No. 09/064,348, filed April 22, 1998, which is a reissue application of U.S. Patent No. 5,514,907, issued May 7, 1996. The parent reissue application (i.e., Serial No. 09/064,348) has now been allowed and the issue fee has been paid. The original U.S. patent in connection with which these reissue applications have been filed is now surrendered. A copy of the Offer to Surrender by the Applicant and Assent of the Assignee, which was filed in the parent reissue application, is submitted herewith. The original patent grant was submitted and surrendered in the patent reissue application.

The foregoing amendment to the specification adds priority data in accordance with 35 U.S.C. § 120 in order to properly reference the parent reissue application. The priority data also references the original patent grant.

By the foregoing amendments, Applicant also cancels original Claims 1-34 (Claims 1-6 and 8-34 having been allowed in the patent reissue application) and adds Claims 35-38. Claims 35-38 correspond to Claims 48-51 in the parent reissue application with some amendments. These claims were canceled in the parent reissue application in order to advance that case toward issuance, and Applicant now files this continuation application in order to pursue these claims.

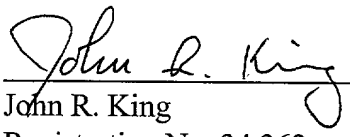
Appl. No.	:	**Unknown**
Filed	:	**Herewith**

Applicant submits herewith a Second Supplemental Reissue Application Declaration relating to the claims submitted in this reissue continuation application. Accordingly, Applicant respectfully requests entry of these amendments before examination by the Examiner on the merits begins.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: February 28, 2000

By: 

John R. King
Registration No. 34,362
Attorney of Record
620 Newport Center Drive
Sixteenth Floor
Newport Beach, CA 92660
(949) 760-0404

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APPARATUS FOR STACKING SEMICONDUCTOR CHIPS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the vertical stacking of conventional integrated circuit packages to increase the density of components on a printed circuit board. More particularly, the present invention relates to the vertical stacking of conventional memory integrated circuits packages on a surface mount printed circuit board.

2. Description of the Related Art

An integrated circuit or "IC" is a microcircuit formed from active and passive electrical components interconnected on or within a single semiconductor substrate. To protect the IC and to facilitate connection of the IC to a printed circuit board, off-the-shelf ICs are commonly packaged within a ceramic, plastic or epoxy IC package having multiple external terminals or "pins." The full integrated circuit package, including the IC, is commonly referred to (and will be referred to herein) as a "chip."

As a result of the continuously increasing demand for large random access computer memories, and the demand for smaller computers, various techniques have been developed to increase densities of memory chips on printed circuit boards. In addition to the inherent size advantages provided, increased chip densities enable shorter circuit paths between components, allowing the components to operate at higher speeds while reducing radio-frequency interference (RFI) and electromagnetic interference (EMI) emitted from the printed circuit board.

One development that has led to a significant increase in memory chip densities has been the advent of surface mount technology. With surface mount technology, conventional plated through holes on printed circuit boards are replaced with conductive pads, and through-hole pins of conventional chips are replaced with smaller surface mount pins. Because the pitch or spacing between centers of adjacent surface mount pins is significantly less than the conventional 0.10-inch spacing for conventional through-hole components, surface mount chips tend to be considerably smaller than corresponding conventional chips, and thus take up less space on the printed circuit board. Surface mount technology additionally facilitates the mounting of components on both sides of the printed circuit board.

Various techniques have been developed for increasing chip densities on printed circuit boards by vertically stacking or "piggybacking" two or more chips. See, for example, U.S. Pat. No. 4,996,583 to Hatada, U.S. Pat. No. 4,398,235 to Lutz et al., U.S. Pat. No. 4,953,005 to Carlson et al., Japanese Patent Publication No. 61-63048 to Toshiba Corp., Japanese Patent Publication No. 58-219757 to Tokyo Shibaura Denki K. K., Japanese Patent Publication No. 61-75558 to NEC Corp., and Japanese Patent Publication No. 60-254762 to Fujitsu. These techniques, however, tend to suffer from a number of defects. For instance, many of the techniques require the manufacture of custom chips that are specifically designed for stacking, or else require special modifications to the pins of standard memory chips. Further, many of the techniques do not make use of the various advantages of surface mount technology, such as the ability to maintain a low-profile when memory chips are mounted to the printed circuit board. Further, many proposed techniques for stacking memory chips are not cost effective.

SUMMARY OF THE INVENTION

The present invention involves a multi-chip memory module having two or more vertically stacked memory chips that are interconnected using a pair of printed circuit boards or "side boards." The multi-chip memory module can be constructed using standard, off-the-shelf memory chips, without modification to the pins of the memory chips. The multi-chip memory module is constructed such that pins of the lower-most memory chip in the stack are surface-mountable directly to pads of a memory board, permitting the multi-chip memory module to be mounted with a low profile relative to the memory board.

In accordance with one aspect of the invention, the multi-chip memory module comprises a plurality of memory chips that are stacked on top of one another, with each memory chip having conductive surface mount pins. First and second side boards are mounted to the stacked memory chips such that the side boards are substantially parallel to one another. Each of the two side boards has vias for receiving the surface mount pins of the memory chips, with the vias arranged in rows such that each row corresponds to a respective memory chip. Vias of a bottom-most row of each side board fall along a lower side board edge, so that vias of the bottom-most row serve as surface mount terminals for surface mounting the multi-chip memory module to pads of a printed circuit board. Conductive traces are provided on or within each side board for interconnecting the surface mount pins of the memory chips.

In accordance with another aspect of the invention, there is provided a memory module that includes at least one multi-chip module. The memory module includes a circuit board having at least first and second sets of surface mount pads. The memory module further includes a first side board that is surface-mounted to the first set of surface mount pads such that the first side board is substantially perpendicular to the circuit board, and a second side board that is surface-mounted to the second set of surface mount pads such that the second side board is substantially perpendicular to the circuit board and substantially parallel to the first side board. The memory module further includes a plurality of chips stacked on top of one another between the side boards, with each chip conductively connected to the first and second side boards.

In accordance with an additional aspect of the invention, there is provided a method of increasing the density of memory chips on a memory board. The method includes the step of providing first and second side boards, with each side board comprising a printed circuit board having vias thereon, and with vias along bottom edges of the side boards forming surface mount terminals. The method further includes the step of stacking a plurality of memory chips on top of one another to generate a stack of memory chips. The method further includes the steps of positioning the first and second side boards relative to the stack of memory chips such that terminals of the memory chips extend within the vias, and attaching the first and second side boards to the stack of memory chips by filling the vias with solder.

In accordance with another aspect of the invention, there is provided a method of interconnecting circuit board components to increase component density. The method includes the step of constructing a first printed circuit board that has a plurality of vias formed along a row. The method further includes the step of cutting the first printed circuit board along the row to expose the vias along an edge of the printed circuit board. The method further includes the steps of soldering the vias to respective pins of a semiconductor chip,

and soldering the vias to pads of a second printed circuit board such that the first printed circuit board is substantially perpendicular to the second printed circuit board.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the invention will now be described with reference to the drawings of a preferred embodiment, which is intended to illustrate and not to limit the invention, and in which:

FIG. **1** is a perspective view illustrating a multi-chip memory module in accordance with a preferred embodiment of the present invention, illustrated above a portion of a printed circuit board to which the multi-chip memory module may be surface mounted. Solder plugs and circuit board traces are omitted to show the construction of the multi-chip memory module;

FIG. **2** is an exploded perspective view of the multi-chip memory module of FIG. **1**;

FIG. **3** is a top plan view of the multi-chip memory module of FIG. **1**, with terminal numbers for the multi-chip memory module shown in brackets;

FIG. **4** is a cross sectional view taken along the line **4**—**4** of FIG. **1**;

FIGS. **5***a* and **5***b* are top and bottom plan views of a portion of a circuit board panel, illustrating a process of manufacturing side boards in accordance with the present invention, and further illustrating conductive traces on first and second sides of the side boards of FIG. **1**;

FIG. **6***a* is an enlarged view in partial cross section, showing a bottom portion of a side board of the multi-chip memory module of FIG. **1** with partially cut-away vias filled with solder to form surface mount terminals, and further showing the printed circuit board and pads of FIG. **1**;

FIG. **6***b* is an enlarged view in partial cross section of a side board and a printed circuit board with pads, illustrating an alternative configuration that results when conductive cylinders of vias are pushed inward during a routing process;

FIG. **7** is a schematic diagram illustrating the electrical interconnections of memory chip pins and side board terminals for the multi-chip memory module of FIG. **1**, with chip pin numbers shown in parenthesis and multi-chip memory module terminal numbers shown in brackets; and

FIG. **8** is a plan view of a single in-line memory module having eight multi-chip memory modules surface mounted to one side thereof.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

In accordance with one embodiment of the present invention, one multi-chip memory module design is described herein. In order to fully specify this preferred design, various embodiment-specific details are set forth, such as the number of memory chips in the module, the layouts of the printed circuit boards of the module, and the capacity, number of data bits and pin-outs of the memory chips. It should be understood, however, that these details are provided only to illustrate this single preferred embodiment, and are not intended to limit the scope of the present invention.

With reference to FIGS. **1**–**4**, a 28-terminal multi-chip memory module **30** (hereinafter "multi-chip module") comprises four functionally-identical, vertically-stacked memory chips **32**, **34**, **36**, **38**. The memory chips **32**–**38** are conventional 24-pin surface mount TSOP ("thin small outline package") chips, available from Toshiba, Mitsubishi,

and the like. Each memory chip **32–38** has a capacity of 16M×1-bit.

The vertically-stacked memory chips **32–38** are held together and electrically interconnected by a pair of printed circuit boards **42, 44**, referred to herein as "side boards." The side boards **42, 44** are positioned in parallel to each other, and perpendicular to the top surfaces of the chips **32–38**. The multi-chip module **30** is configured to be surface-mounted to a memory board **70** (FIG. **1**) that has surface mount pads **66** thereon.

As used herein to describe the multi-chip module **30**, the term "bottom" refers generally to the portion of the multi-chip module **30** that is closest to the memory board **70** when the multi-chip module **30** is mounted to the memory board **70**. The terms "top," "bottom," and "lower" are not intended to imply a specific spacial orientation of the multi-chip module **30**.

Each side board **42, 44** has a plurality of plated through-holes or "vias" **48** for receiving the pins **50** of the chips **32–38**, with each via **48** comprising a conductive tubular cylinder portion **48***a* that extends through the side board. The vias **48** are positioned to form four horizontal rows **52, 54, 56, 58**, with each row corresponding to a respective memory chip **32, 34, 36, 38**. With reference to FIG. **4**, the rows **52–58** of vias are formed such that the distance D between centers of adjacent rows is approximately equal to the thickness T of each chip **32–38**, so that adjacent memory chips are touching (or nearly touching) each other when the multi-chip module **30** is assembled. This close spacing of adjacent memory chips contributes to a low profile of the multi-chip module **30** relative to the memory board **70** (FIG. **1**), as further discussed below. Adjacent memory chips could alternatively be spaced apart from one another, as may be desirable in certain applications to facilitate the cooling of the memory chips **32–38**.

With reference to FIGS. **1** and **2**, for each side board **42, 44**, the vias of the bottom-most row **58** are partially cut away, with the conductive cylinder **48***a* of each such via extending to the lower edge **80** of the side board so that the pins **50** of the bottom-most chip **38** can be soldered directly to the surface mount pads **66** (FIG. **1**) of the memory board **70**. The vias **48** along the lower edges **80** of the side boards **42, 44** thus serve as surface mount terminals. This aspect of the multi-chip module **30**, in combination with the close spacings between adjacent memory chips, allows the multi-chip module **30** to be mounted with a very low profile relative to the memory board **70**. The lower edge **80** is preferably formed using a routing machine, as further described below. As illustrated in FIG. **3**, the multi-chip module **30** has a total of 28 surface mount terminals (terminal numbers shown in brackets), with the terminals arranged in two rows of 14 terminals each.

With reference to FIG. **1**, the surface mount pads **66** are arranged in two rows of 14 pads each (corresponding to the 14 terminals per side board **42, 44**), with the distance between the two rows corresponding to the width of each chip **32–38**. As best seen in FIGS. **1** and **3**, the multi-chip module **30** occupies approximately the same area on the memory board **70** as would a single one of the memory chips **32–38**.

Conductive traces (shown in FIGS. *5a* and *5b*) of the side boards **42, 44** interconnect the pins **50** of the memory chips **32–38** such that all memory locations of all memory chips **32–38** can be utilized. In the embodiment shown, the memory chips **32–38** are interconnected such that all four 16M× 1-bit chips **32–38** are selected simultaneously, with

each chip supplying (or, during a write cycle, storing) one bit of data. The multi-chip module **30** thus acts as a 16M×4-bit memory module.

With reference to FIGS. **1–3**, four "extra" vias **72** are provided along the lower edges **80** of the multi-chip module **30**. The four vias **72** serve as terminals only, and do not receive pins **50** of any of the memory chips **32–38**. Each via **72** provides access to either a data input pin or a data output pin of a respective memory chip **32–38**, and is thus dedicated to a single chip. It will be recognized that other types of terminal structures could be used in place of the vias **72**.

To assemble the multi-chip module **30**, the memory chips **32–38** are initially stacked on top of one another. The side boards **42, 44** are then positioned so that the pins **50** extend within the corresponding vias, as best shown by FIG. **4**. Advantageously, no modification to the pins **50** of the standard TSOP memory chips **32–38** is required. Once the side boards **42, 44** are properly positioned, all of the vias **48** of both side boards **42, 44** are filled with solder (solder plugs omitted in FIGS. **1–4**). A solder with a relatively high melting point is used for this purpose so that the multi-chip module **30** can subsequently be mounted to the memory board **70** using a solder with a lower melting point without melting the solder within the vias **48**.

A preferred process for manufacturing the side boards **42, 44** of the multi-chip module **30** will now be described with reference to FIGS. **5***a* and **5***b*, which illustrate a circuit board panel **90** mid-way through the manufacturing process. FIG. **5***a* illustrates the outward-facing surface (relative to the multi-chip module **30**) of the side board **42**, and the inward-facing surface of the side board **44**. FIG. **5***b* illustrates the inward-facing surface of the side board **42**, and the outward-facing surface of the side board **44**.

Traces **92** are initially formed on both sides of the circuit board panel **90** using a conventional film etching process. Via holes are then drilled through the circuit board panel **90**, with the holes positioned to correspond to the pin positions of the chips **32–38**. A conventional plating process is then used to form the conductive cylinders **48***a* of the vias **48** (preferably formed from copper), and to interconnect the via cylinders **48***a* to the appropriate traces **92**.

Once the vias **48** and traces **92** are formed, the panel **90** is routed to form the lower edge **80** and the top edge **81** of each side board **42, 44**. The panel **90** shown in FIGS. **5***a* and **5***b* is mid-way through the routing process, with top and bottom edges **80, 81** formed only for the four side boards **42, 44** closest to the bottom of each Figure. During the routing process, the routing bit is preferably passed so that approximately 5% of the diameter of each via cylinder **48***a* along the bottom row **58** is cut away. Due to imperfections in the routing process, the lower portions of some cylinders may be pushed inward (toward the centers of the respective vias) by the routing bit, as schematically shown at **96** in FIGS. **5***a* and **5***b* (and further illustrated in FIG. **6***b*). Cylinders that are formed in this manner have been found to work well as surface mount terminals, and need not be modified.

The panel **90** is scored on both sides to form break-away grooves **94**. The break-away grooves **94** can be formed either before or after the above-described routing process. Finally, side boards **42, 44** are manually broken away from the panel **90**, and soldered to stacks of memory chips (as described above) to form multi-chip modules **30**.

With reference to FIG. **6***a*, once the partially cut-away vias **48** along the bottom edge **80** of a side board **42, 44** are filled with solder, a portion of each solder plug **98** is exposed along the bottom edge **80**, forming a terminal that can be

soldered to a corresponding surface mount pad **66**. Each solder plug **98** preferably extends slightly below the lower edge **80**, facilitating connection of the multi-chip module **30** to the pads **66**. As illustrated in FIG. **6***b*, via cylinders **48***a* that are pushed inward during the routing process are similarly exposed along the lower edge **80**, and are well-suited for connection to the pads **66**.

FIG. **7** illustrates the interconnections the memory chips **32–38** of the multi-chip module **30**, and also illustrates the connections between the memory chips **32–38** and the 28 terminals of the multi-chip module **30**. Signal names for each of the 28 multi-multi-chip module terminals are shown at the left of FIG. **7**. Terminal numbers for the multi-chip module **30** are shown in brackets in FIG. **7**, and correspond to the bracketed terminal numbers of FIG. **3**. Pin numbers for the chips **32–38** are shown in parenthesis in FIG. **6**. As shown, like address pins (A0–A11), control pins (RAS, CAS and WE), and power pins (VCC and VSS) of the four memory chips **32–38** are connected together, and are connected to respective terminals of the multi-chip module **30**. For example, the A0 pins (pin **8**) of all four memory chips **32–38** are connected together, and are accessed via terminal **10** of the multi-chip module. With like address and control pins connected together, all four chips **32–38** are selected simultaneously, and are fed identical address values. The data-input pin (D) of each memory chip **32–38** is connected to a respective dedicated input terminal (D0–D3) of the multi-chip module **30**, allowing a 4-bit value to be written to the multi-chip module **30** on each write cycle. Similarly, the data-output pin (Q) of each memory chip **32–38** is connected to a respective dedicated output terminal (Q0–Q3), allowing a 4-bit value to be read from to the multi-chip module **30** on each read cycle. As will be recognized, the chips **32–38** could alternatively be connected such that fewer than all of the chips are selected with each multi-chip module access. For example, a 64M×4-bit multi-chip module can be constructed from four 16M×4-bit memory chips that are interconnected so that only one memory chip is selected at a time. In such an arrangement, the write enable pins and like address, data-in, and data-out pins of all four memory chips would be connected, and the RAS and CAS pins of each chip would be connected to dedicated RAS and CAS input lines (i.e., one pair of RAS/CAS input lines per memory chip).

FIG. **8** illustrates one side of a 16M×36 bit single in-line memory module (SIMM) **100** in accordance with the present invention. The SIMM **100** comprises a SIMM board **170** having eight 16M×4 bit multi-chip modules **30***a*–**30***h* mounted on the side shown. Four 16M×1-bit TSOP memory chips (not shown) are mounted on the opposite side of the SIMM board **170**, in addition to one or more conventional buffer chips. Standard connector terminals **104** are provided along the bottom edge of the SIMM **100**, permitting insertion of the SIMM into a connector slot. The eight 16M×4-bit multi-chip modules **30***a*–**30***h* and four 16M×1-bit memory chips combine to produce a data width of 36 bits (32 data bits plus 4 error-correction code bits). The low profile of each multi-chip module **30***a*–**30***h* advantageously enables multiple SIMMs to be mounted in close proximity to one another within a computer.

While the design of a single multi-chip module **30** has been described in detail herein, various modifications to the design are possible without departing from the scope of the present invention. For example, a different type of memory chip can be used in the place of the 16M×1-bit chips **32–38** of the multi-chip module **30**. Alternatively, a mixture of memory chips of different types can be used. Further, a different number of chips per multi-chip module can be

used. Further, the side boards **42, 44** may be constructed according to alternative techniques that are apparent to those skilled in the art.

It will further be noted that the stacking techniques described herein may be useful in alternative applications that do not involve the stacking of memory chips. For example, the stacking techniques could be used to stack multiple buffer chips, or to stack multiple logic driver chips.

Accordingly, the scope of the present invention is intended to be defined only by reference to the appended claims.

What is claimed is:

1. A multi-chip memory module, comprising:

a plurality of memory chips stacked on top of one another, each memory chip of said plurality having conductive surface mount pins; and

first and second side boards mounted to said memory chips such that said side boards are substantially parallel to one another, each side board having:

vias for receiving said surface mount pins of said memory chips, said vias arranged in rows such that each row corresponds to a respective memory chip of said plurality, vias of a bottom-most row receiving surface mount pins of a bottom-most memory chip of said plurality, said bottom-most row falling along a lower side board edge such that vias of said bottom-most row serve as surface mount terminals for surface mounting the multi-chip memory module to pads of a printed circuit board; and

conductive traces for interconnecting said vias.

2. A multi-chip memory module as defined in claim **1**, wherein said vias of said bottom-most row are exposed along said lower side board edge.

3. A multi-chip memory module as defined in claim **1**, wherein all memory chips of said plurality are functionally identical.

4. A multi-chip memory module as defined in claim **1**, wherein the total number of surface mount terminals on said first and second side boards is greater than the number of said surface mount pins on any one of said plurality memory chips.

5. A multi-chip memory module as defined in claim **1**, wherein said memory chips of said plurality are interconnected by said traces such that all memory chips of said plurality are selected simultaneously.

6. A multi-chip memory module as defined in claim **1**, in combination with a memory board having surface mount pads thereon, said vias of said bottom-most row soldered to said surface mount pads.

7. A module that includes at least one multi-chip module, said module comprising:

a circuit board having at least first and second sets of surface mount pads;

a first planar side board including a plurality of surface mount contacts positioned along an edge of said first side board which abuts said circuit board, said plurality of surface mount contacts of said first side board being surface-mounted to said first set of surface mount pads of said circuit board such that said first side board is substantially perpendicular to said circuit board;

a second planar side board including a plurality of surface mount contacts positioned along an edge of said second side board which abuts said circuit board, said plurality of surface mount contacts of said second side board being surface-mounted to said second set of surface mount pads of said circuit board such that said second side board is substantially perpendicular to said circuit board and substantially parallel to said first side board; and

a plurality of standard surface mount chips stacked between said side boards, each chip including a plurality of pins, a portion of each pin extending beyond a chip surface which lies generally parallel to said circuit board with said chip positioned between said side boards, each chip of said plurality conductively connected to said first side board and said second side board.

8. A module as defined in claim **7**, wherein said first and second sets of surface mount pads are arranged in respective first and second rows.

9. A module as defined in claim **7**, wherein a surface area of a region between said first and second side boards on said circuit board is generally equal to a surface area occupied by one of said chips of said plurality.

10. A module as defined in claim **7**, wherein said standard surface mount chips of said plurality are stacked on top of one another.

11. A module as defined in claim **7**, wherein all chips of said plurality are functionally identical.

12. A module as defined in claim **7**, wherein a lower-most chip of said plurality is soldered to said first and second sets of surface mount pads.

13. A module as defined in claim **7**, wherein each chip of said plurality is a memory chip.

14. A module as defined in claim **12**, wherein said lower-most chip is additionally soldered to vias of said first and second side boards.

15. A module as defined in claim **14**, wherein said lower-most chip is soldered to said vias with a first solder that has a first melting point, and is soldered to said first and second sets of surface mount pads with a second solder that has a second melting point, said second melting point lower than said first melting point.

16. A multi-chip module comprising:

first and second support structures, each support structure including a plurality of electrically conductive paths and a plurality of surface mount contacts positioned along an edge thereof, the plurality of surface mount contacts arranged to align with corresponding surface mount pads on a printed circuit board to electrically couple the first and second support structures to the printed circuit board; and

at least first and second juxtaposed standard surface mount chips, each chip having planar surfaces extending between at least a pair of sides of the chip, the planar surfaces arranged generally between the support structures with the planar surfaces of adjacent chips positioned face to face, each side of each chip including a plurality of pins extending toward one of the support structures beyond the side, at least some of the pins being electrically connected to one of the support structures.

17. The multi-chip module of Claim 16, wherein the juxtaposed standard surface mount chips are functionally identical.

18. The multi-chip module of Claim 16, wherein the juxtaposed standard surface mount chips are interconnected by the plurality of electrically conductive paths such that all of the juxtaposed standard surface mount chips may be selected simultaneously.

19. The multi-chip module of Claim 16, wherein the electrical conductive paths are electrically coupled to at least some of the pins of the juxtaposed standard surface mount chips and are arranged so as to individually select at least one of the juxtaposed standard surface mount chips.

20. The multi-chip module of Claim 16, wherein a total number of the surface mount contacts is greater than the total number of pins of the first chip.

21. The multi-chip module of Claim 16, wherein at least some of the pins of the juxtaposed standard surface mount chips are mechanically connected to one of the support structures.

22. The multi-chip module of Claim 21, wherein the plurality of pins associated with a lower-most one of the juxtaposed standard surface mount chips are attached to at least some of the plurality of surface mount contacts.

23. The multi-chip module of Claim 16, wherein at least some of the pins of the juxtaposed standard surface mount chips are solder connected to one of the support structures so as to mechanically and electrically connect the pins to the support structures.

24. The multi-chip module of Claim 16, wherein all of the juxtaposed standard surface mount chips of the module are positioned to lie entirely between the first and second support structures.

25. The multi-chip module of Claim 16, wherein at least corresponding portions of the first and second support structures lie generally parallel to each other.

26. The multi-chip module of Claim 25, wherein the first and second support structures comprise planar side boards.

27. The multi-chip module of Claim 25, wherein each of the first and second support structures extends along at least a side of one of the plurality of juxtaposed standard surface mount chips.

28. The multi-chip module of Claim 27, wherein each support structure has a unitary construction.

29. The multi-chip module of Claim 25, wherein the planar surfaces of each chip lie generally normal to the parallel corresponding portions of the first and second support structures.

30. The multi-chip module of Claim 16, wherein the first standard surface mount chip is aligned above the second standard surface mount chip.

31. The multi-chip module of Claim 16, wherein the first and second support structures comprise opposing inner surfaces, and the pins of the juxtaposed standard surface mount chips extend outward beyond the inner surfaces of the first and second support structures.

32. The multi-chip module of Claim 31, wherein said first and second support structures each include a plurality of vias that are arranged to receive at least outer ends of at least some of the pins.

33. The multi-chip module of Claim 16, wherein the first and second support structures are spaced apart from each other by a distance less than a distance between an outer end of a first pin on one side of the first standard surface mount chip and an outer end of a second pin on an opposite side of the first standard surface mount chip.

34. The multi-chip module of Claim 16, wherein said planar surfaces of each chip lies generally within respective parallel planes, and each pin of at least one of the chips connects the corresponding support structure at a location outside the space between the planes.

APPARATUS FOR STACKING SEMICONDUCTOR CHIPS

Abstract of Disclosure

A multi-chip memory module comprises multiple standard, surface-mount-type memory chips stacked on top of each other, and a pair of printed circuit boards mounted on opposite sides of the memory chips to electrically interconnect the memory chips. Each printed circuit board has vias that are positioned to form multiple rows, with each row of vias used to connect the printed circuit board to a respective memory chip. The vias falling along the bottom-most row of each printed circuit board are also exposed and are used to surface mount the multi-chip module to pads of a memory board.

SIMTECH.088RA

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Mark Moshayedi
Assignee	:	SIMPLE TECHNOLOGY INCORPORATED
Reissue of Patent No.	:	5,514,907
Issued	:	May 7, 1996
For	:	APPARATUS FOR STACKING SEMICONDUCTOR CHIPS

REISSUE APPLICATION DECLARATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, as a named inventor, declare as follows:

1. I am a citizen of the United States. My residence and post office address are 2019 Hillside Drive, Orange, California 92669.

2. I believe that I am an original, first and sole inventor of the subject matter described and claimed in U.S. Patent No. 5,514,907 ("the '907 patent"), issued May 7, 1996, and of the subject matter disclosed and claimed in the accompanying reissue application.

3. I have reviewed and understand the contents of the specification of the accompanying reissue application.

4. I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56. In compliance with this duty and in accordance with 37 CFR 1.97-1.98, an Information Disclosure Statement is being submitted with the reissue application.

5. On information and belief, U.S. Patent No. 5,514,907 is partially inoperable by claiming less that I had a right to claim. Specifically, the insufficiency in the claims resides in the failure to present claims directed to a set of support structures including a plurality of surface mount contacts and a plurality of juxtaposed standard surface mount chips extending between the support structures and arranged with planar surfaces of adjacent chips positioned face to face. The new claims presented in the reissue application are directed to this feature, while the original claims of the '907 patent are not.

6. Turning from the unclaimed subject matter at large to a specific reissue claim, the reissue application includes one new independent claim: Claim 16. The newly claimed subject matter of Claim16 is best understood by a comparison with original Claim 7 of the '907 patent. Presented below is a mock claim which illustrates the claim language common to Claims 7 and 16 in plain type, the claim language specific to Claim 7 in bracketed type, and the claim language specific to Claim 16 in underlined type:

> A [module that includes at least one] multi-chip module[, said module] comprising:
>
> [a circuit board having at least first and second sets of surface mount pads;]
>
> [a first planar side board] <u>first and second support structures, each support structure</u> including <u>a plurality of electrically conductive paths and</u> a plurality of surface mount contacts positioned along an edge <u>thereof, the plurality of surface</u>

mount contacts arranged to align with corresponding surface mount pads on a printed circuit board to electrically couple the first and second support structures to the printed circuit board [of said first side board which abuts said circuit board, said plurality of surface mount contacts of said first side board being surface-mounted to said first set of surface mount pads of said circuit board such that said first side board is substantially perpendicular to said circuit board];

[a second planar side board including a plurality of surface mount contacts positioned along an edge of said second side board which abuts said circuit board, said plurality of surface mount contacts of said second side board being surface-mounted to said second set of surface mount pads of said circuit board such that said second side board is substantially perpendicular to said circuit board and substantially parallel to said first side board;] and

[a plurality of] at least first and second juxtaposed standard surface mount chips, each chip having planar surfaces extending between at least a pair of sides of the chip, the planar surfaces arranged generally between the support structures with the planar surfaces of adjacent chips positioned face to face, [stacked between said side boards,] each side of each chip including a plurality of pins[, a portion of each pin] extending toward one of the support structures beyond the side, [a chip surface which lies generally parallel to said circuit board with said chip positioned between said side boards, each chip of said plurality conductively connected to said first side board and said second side board] at least some of the pins being electrically connected to one of the support structures.

The above illustration clearly identifies the differences in the claimed subject matter and evidences the difference in scope between Claim 7 and reissue Claim 16. No original claim has a scope equal to that defined by reissue Claim 16.

7. On information and belief, all errors being corrected in the reissue application arose without any deceptive intent on the part of the Applicant.

I have read and understand the foregoing statements of this Declaration. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or patent issuing therefrom.

Dated: 4-20-98 By: _____
Mark Moshayedi

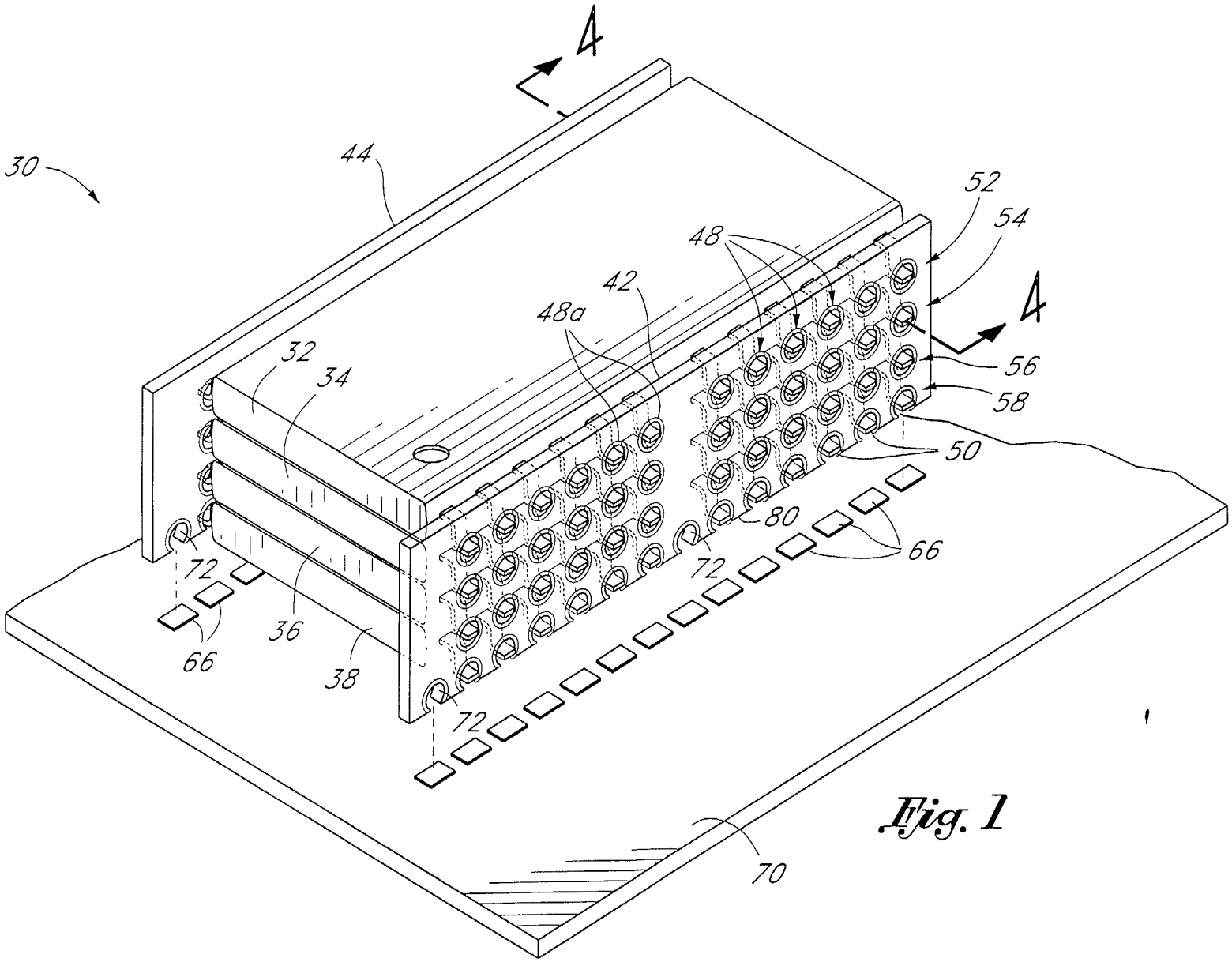

Fig. 1

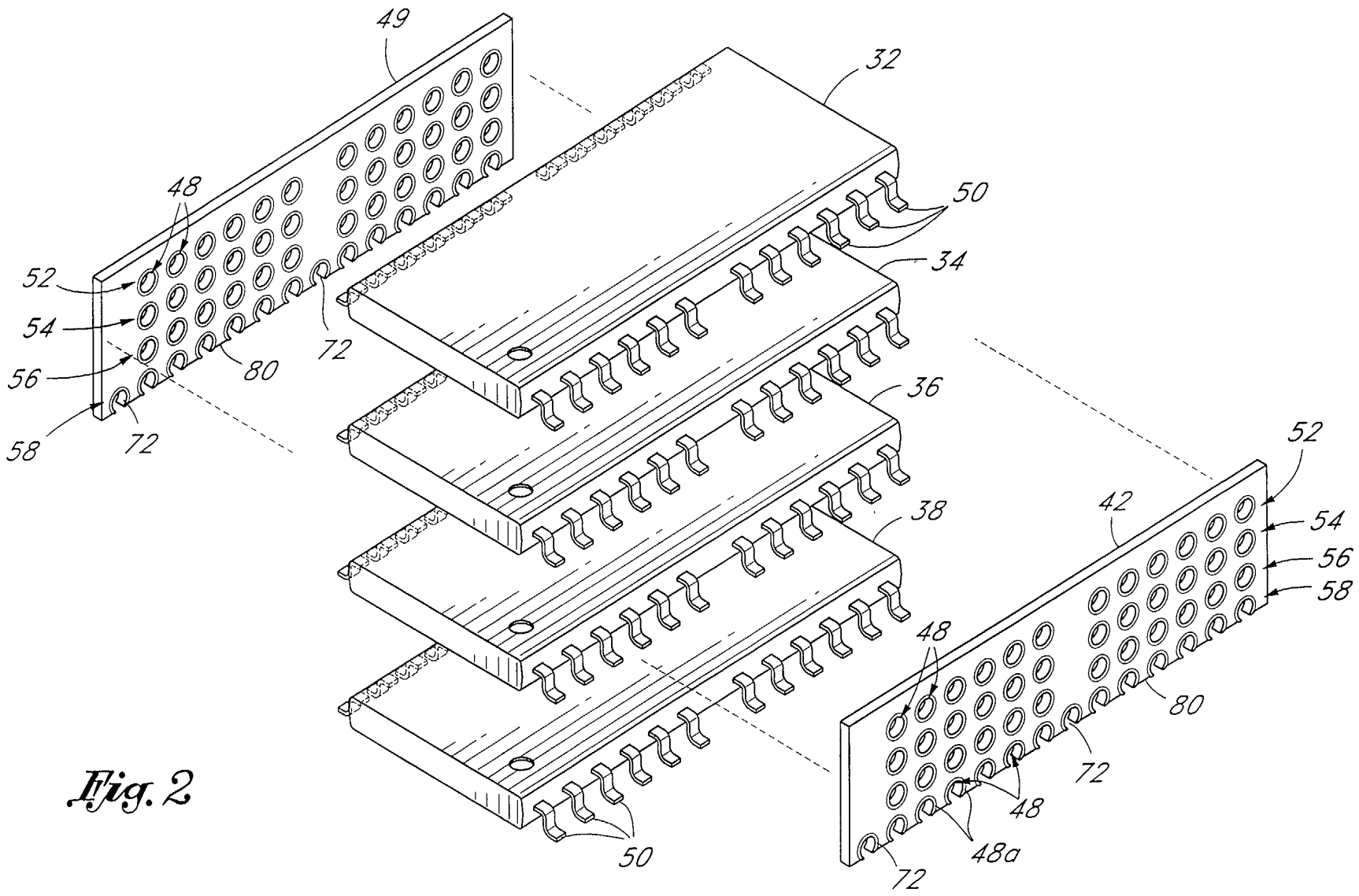

Fig. 2

Fig. 3

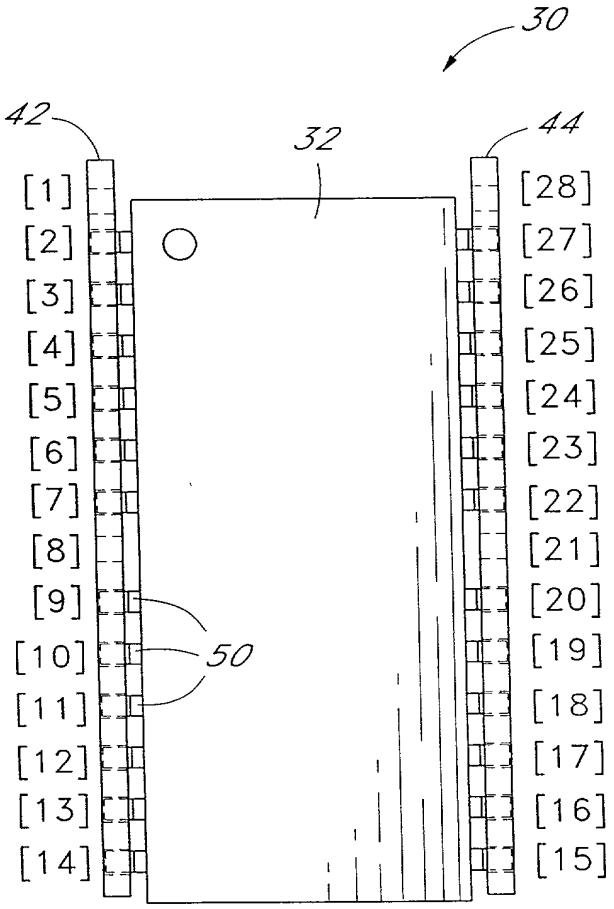
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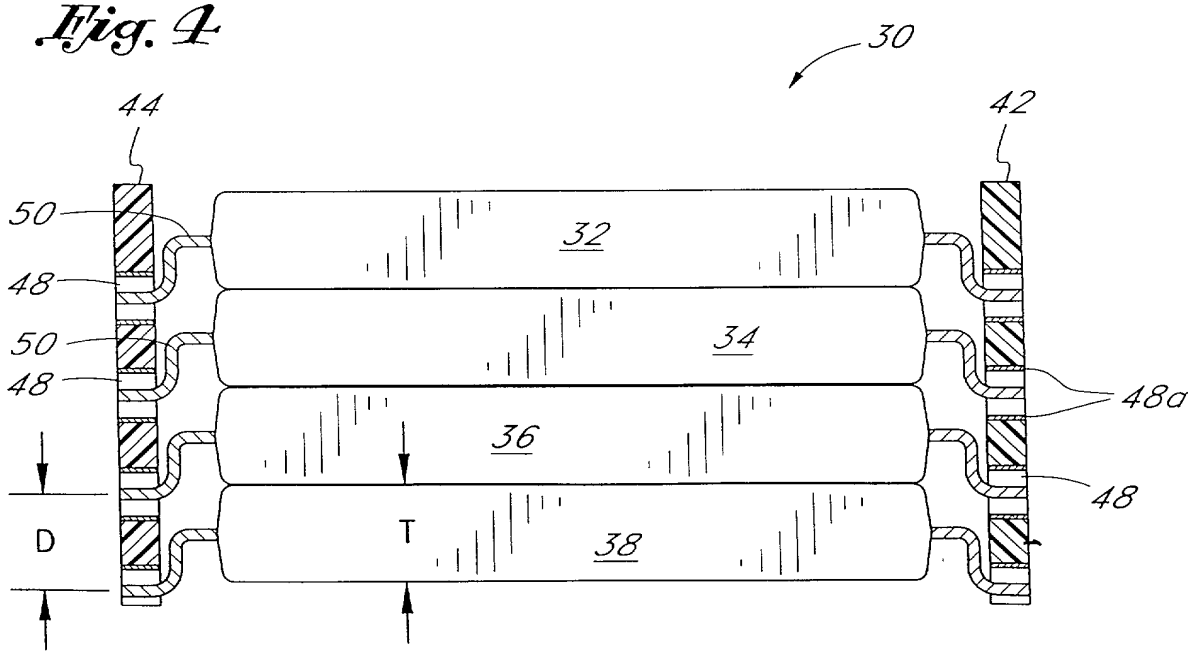
Fig. 4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48

Fig. 5a

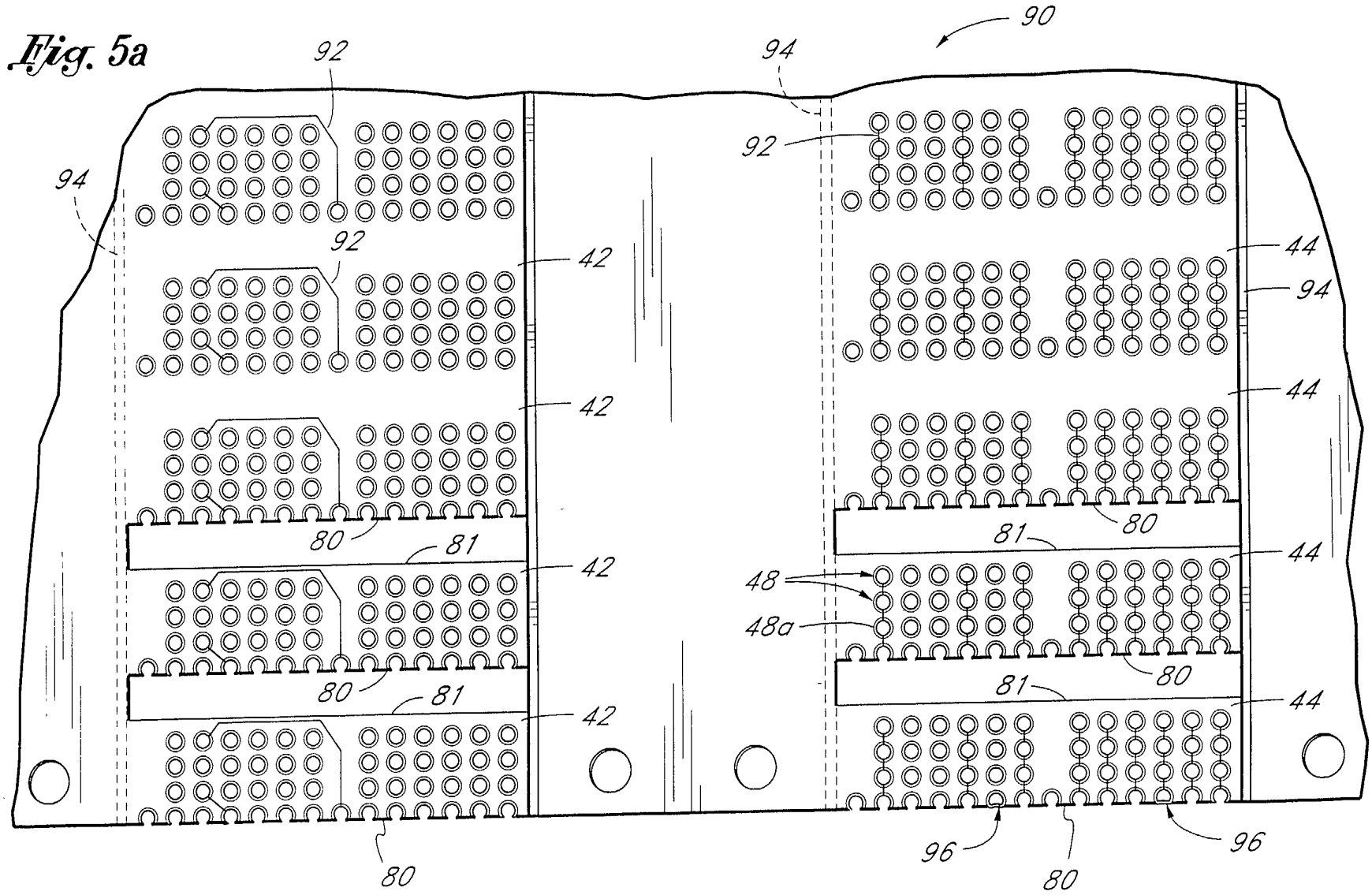
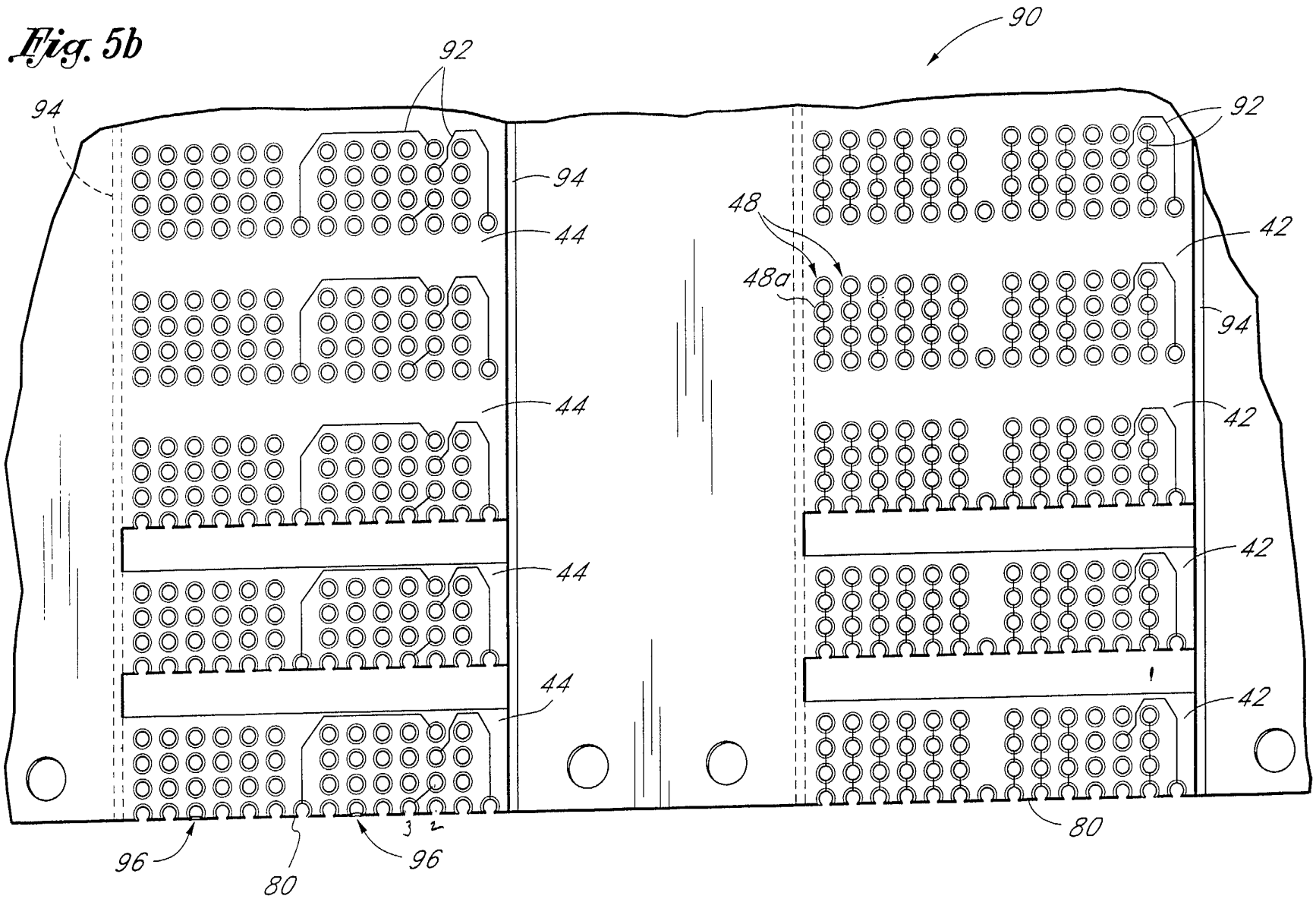


Fig. 5b



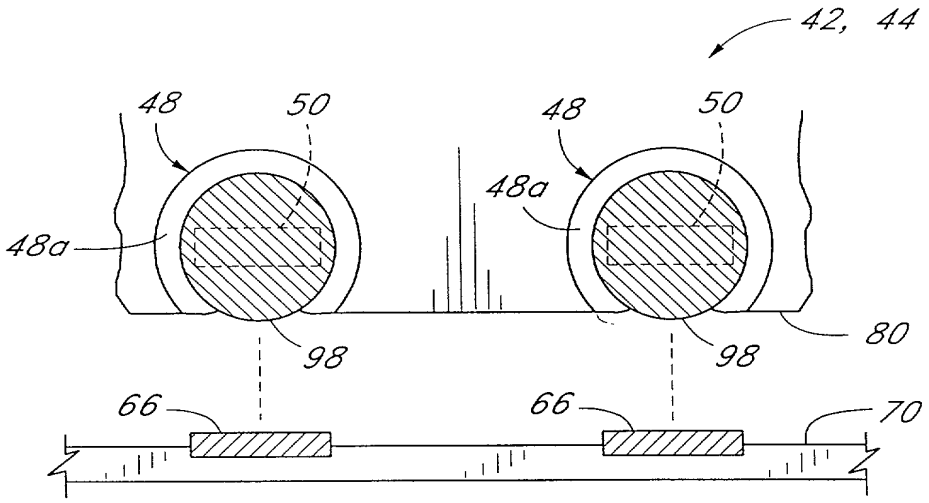

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Fig. 6a

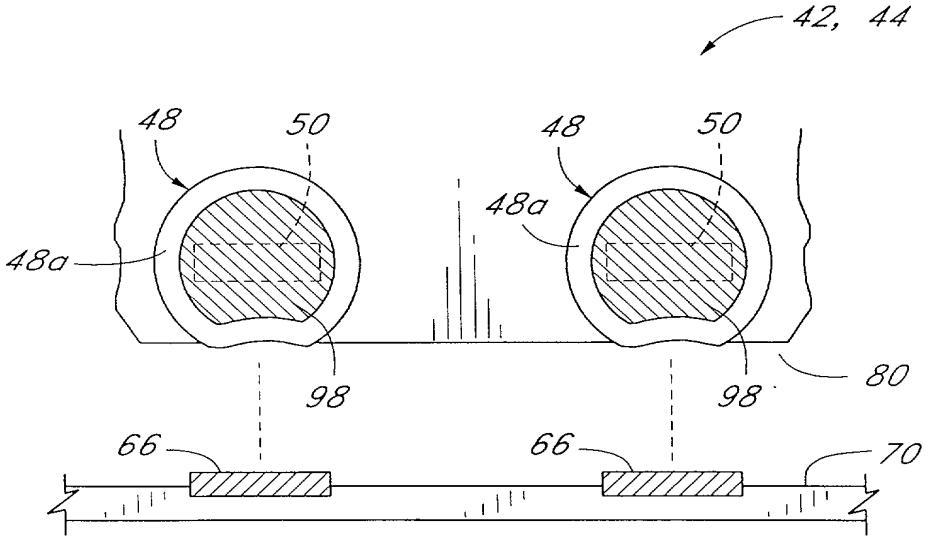
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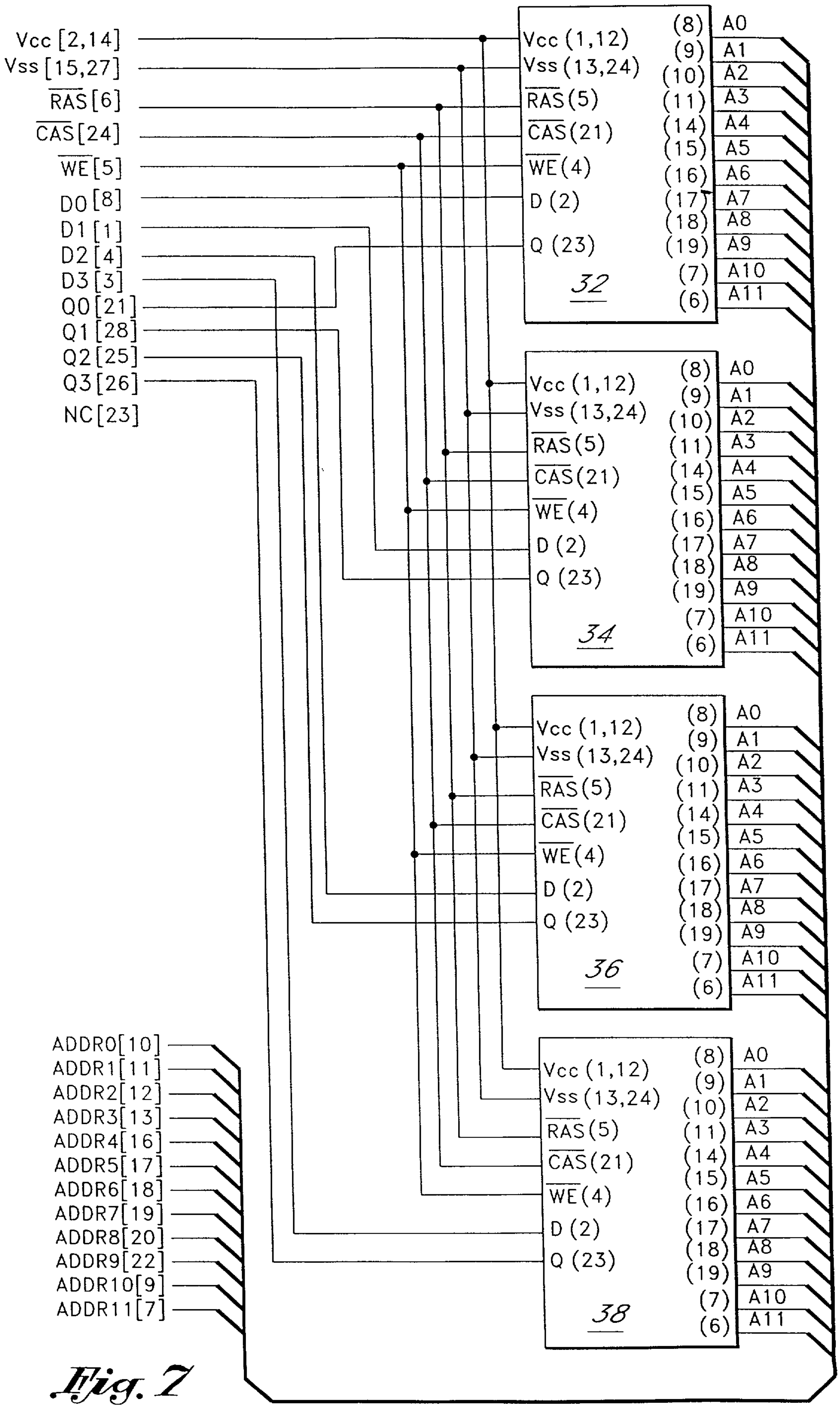
Fig. 6b



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Vss [15,27]
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D2 [4]
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Vss (13,24)
RAS (5)
CAS (21)
WE (4)
D (2)
Q (23)
(8) A0
(9) A1
(10) A2
(11) A3
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Fig. 7

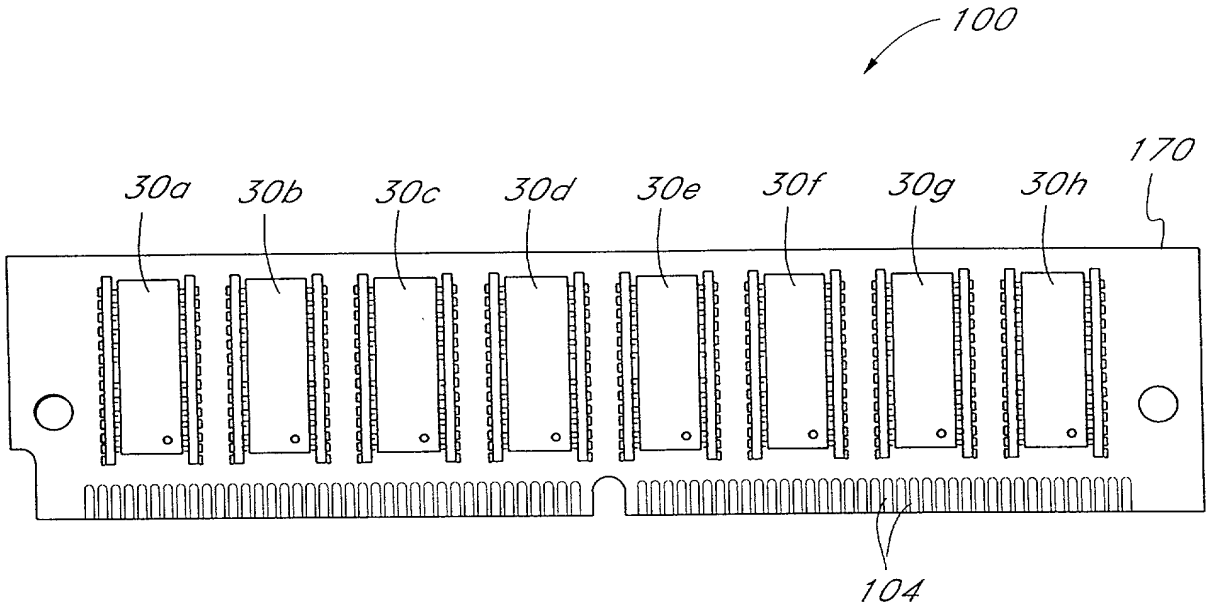

Fig. 8

SIMTECH.088RA PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Mark Moshayedi
App. No.	:	Unknown
Filed	:	Herewith
For	:	APPARATUS FOR STACKING SEMI CONDUCTOR CHIPS
Examiner	:	Unknown

ESTABLISHMENT OF RIGHT OF ASSIGNEE TO TAKE ACTION AND REVOCATION AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned is empowered to act on behalf of the assignee below (the "Assignee"). A true copy of the original Assignment of the above-captioned application from the inventor(s) to the Assignee is attached hereto. This Assignment represents the entire chain of title of this invention from the Inventor(s) to the Assignee.

I declare that all statements made herein are true, and that all statements made upon information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that willful, false statements may jeopardize the validity of the application, or any patent issuing thereon.

The undersigned hereby revokes any previous powers of attorney in the subject application, and hereby appoints the registrants of Knobbe, Martens, Olson & Bear, LLP, 620 Newport Center Drive, Sixteenth Floor, Newport Beach, California 92660, Telephone (714)

App. No. : Unknown
Filed : Herewith

760-0404, **Customer No. 20,995**, as its attorneys with full power of substitution and revocation to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith. This appointment is to be to the exclusion of the inventor(s) and his attorney(s) in accordance with the provisions of 37 C.F.R. § 3.71.

Please use Customer No. 20,995 for all communications.

SIMPLE TECHNOLOGY INCORPORATED

Dated: 4/20/98

By: _____
Mark Moshayedi

Title: President

Address 3001 Daimler Street
Santa Ana, California 92705

WHS-2315:lcb
041498

Nr 408552

Serial No.: Unknown
Filing Date: Herewith

COPY

PATENT
Client Code: SIMTECH.019A
Page 1

ASSIGNMENT

WHEREAS, I, Mark Moshayedi, a United States citizen, residing at 20191 Hillside Drive, Orange, California 92669, have invented certain new and useful improvements in a METHOD AND APPARATUS FOR STACKING SEMICONDUCTOR CHIPS for which I have executed an application for Letters Patent in the United States, on even date herewith;

AND WHEREAS, Simple Technology Incorporated, a California Corporation, with its principal place of business at 3001 Daimler Street, Santa Ana, California 92705, desires to acquire the entire right, title, and interest in and to the said improvements and the said Application:

NOW, THEREFORE, in consideration of the sum of One Dollar ($1.00) to me in hand paid, and other good and valuable consideration, the receipt of which is hereby acknowledged, I, the said inventor, do hereby acknowledge that I have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto the said Simple Technology Incorporated, its successors, legal representatives and assigns, the entire right, title, and interest throughout the world in, to and under the said improvements, and the said application and all divisions, renewals and continuations thereof, and all Letters Patent of the United States which may be granted thereon and all reissues and extensions thereof, and all rights of priority under International Conventions and applications for Letters Patent which may hereafter be filed for said improvements in any country or countries foreign to the United States, and all Letters Patent which may be granted for said improvements in any country or countries foreign to the United States and all extensions, renewals and reissues thereof; and I hereby authorize and request the Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said improvements to the said Simple Technology Incorporated, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND I HEREBY covenant and agree that I will communicate to the said Simple Technology Incorporated, its successors, legal representatives and assigns, any facts known to me respecting said improvements, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing and reissue applications, make all rightful oaths and generally do everything possible to aid the said Simple Technology Incorporated, its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said improvements in all countries.

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 20 day of March 1995

Mark Moshayedi

STATE OF

COUNTY OF ss.

On March 20, 1995, before me, Mark Moshayedi, personally appeared Mark Moshayedi personally known to me (or proved to me on the basis of satisfactory evidence) to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

[SEAL]

Vicki L. Morrison
Signature

VICKI L. MORRISON
COMM. # 1040406
Notary Public — California
ORANGE COUNTY
My Comm. Expires SEP 30, 1998

WHS-6264 rdt
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TRADEMARK
OFFICE

REEL 1422 FRAME 0821

SIMTECH.088RAC PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Mark Moshayedi
Assignee	:	SIMPLE TECHNOLOGY INCORPORATED
Reissue of Patent No.	:	5,514,907
Issued	:	May 7, 1996
For	:	APPARATUS FOR STACKING SEMICONDUCTOR CHIPS

SECOND SUPPLEMENTAL REISSUE APPLICATION DECLARATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, as a named inventor, declare as follows:

1. I believe I am an original, first and sole inventor of the subject matter described and claimed in Application Serial No. 09/064,348, which is a reissue application of U.S. Patent No. 5,514,907 ("the '907 patent"), now surrendered. I also believe I am an original, first and sole inventor of the subject matter described and claimed in the accompanying application, which is a continuation of co-pending Application Serial No. 09/064,348, and which is being amended by the accompanying Preliminary Amendment filed on even date herewith.

2. I hereby state that I have reviewed and understand the contents of the above identified application, including the specification and claims, as amended by any amendments referred to above.

3. Every error in the patent which is being corrected by the present reissue application, and which is not covered by the prior declarations, arose without any deceptive intention on the part of the applicant.

I have read and understand the foregoing statements of this Declaration. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or patent issuing therefrom.

Dated: 2-27-00 By: _____
Mark Moshayedi

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SIMTECH.088RA PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Mark Moshayedi
Assignee	:	SIMPLE TECHNOLOGY INCORPORATED
Reissue of Patent No.	:	5,514,907
Issued	:	May 7, 1996
For	:	APPARATUS FOR STACKING SEMICONDUCTOR CHIPS

SUPPLEMENTAL REISSUE APPLICATION DECLARATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, as a named inventor, declare as follows:

1. I believe I am an original, first and sole inventor of the subject matter described and claimed in U.S. Patent No. 5,514,907 ("the '907 patent"), issued May 7, 1996, for which reissue is being sought.

2. I also believe I am the original, first and sole inventor of the subject matter which is claimed and for which a reissue patent is sought on the invention entitled APPARATUS FOR STACKING SEMICONDUCTOR CHIPS; the specification of which was filed on April 22, 1998 as Application Serial No. 09/064,348; which amended the '907 patent to include additional claims; and which is being amended by the accompanying Amendment filed on even date herewith.

3. I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendments referred to above.

4. Every error in the patent which is being corrected by the present reissue application, and which is not covered by the prior declaration, arose without any deceptive intention on the part of the applicant.

I have read and understand the foregoing statements of this Declaration. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or patent issuing therefrom.

Dated: 6/25/99 By: _____
Mark Moshayedi

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PATENT

Docket No.: **SIMTECH.088RA**

Date: December 1, 1998

REISSUE APPLICATION BY THE INVENTOR, OFFER TO SURRENDER (37 CFR 1.178)

TO THE COMMISSIONER OF PATENTS AND TRADEMARKS:

The undersigned applicant of the accompanying application for the reissue of letters patent for the improvement in **APPARATUS FOR STACKING SEMICONDUCTOR SHIPS**, U.S. Patent No. **5,514,907**, issued on **May 7, 1996**, of which **Simple Technology Incorporated** is the sole owner by assignment, and on whose behalf and with whose assent the reissue application, Serial No. **09/064,348**, filed **April 22, 1998**, is made, hereby offers to surrender said letter patent.

APPLICANT

Dated: Dec-1-1998

Mark Moshayedi

ASSENT OF ASSIGNEE TO REISSUE

The undersigned is empowered to act on behalf of the assignee, **SIMPLE TECHNOLOGY INCORPORATED** ("Assignee").

In accordance with 37 CFR 3.37(b), Assignee represents that it is the assignee of the entire right, title and interest in the above-identified letters patent by virtue of an assignment from the inventor of said letters patent. The assignment was recorded in the U.S. Patent and Trademark Office at Reel **7422**, Frame **0821**. A copy of the assignment is attached.

The undersigned has reviewed all the documents in the chain of title of the letters patent identified above, and to the best of the undersigned's knowledge and belief, title is in the Assignee.

Assignee hereby assents to the accompanying application for reissue of the above-identified letters patent.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or patent issuing therefrom.

SIMPLE TECHNOLOGY INCORPORATED

Dated: December 1, 1998

Manouch Moshayedi
Chief Executive Officer

KNOBBE, MARTENS, OLSON & BEAR, LLP
620 NEWPORT CENTER DR 16TH FLOOR NEWPORT BEACH, CA 92660
(949) 760-0404 FAX (949) 760-9502

408552

Serial No.: Unknown
Filing Date: Herewith

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PATENT
Client Code: SIMTECH.019A
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ASSIGNMENT

WHEREAS, I, Mark Moshayedi, a United States citizen, residing at 20191 Hillside Drive, Orange, California 92669, have invented certain new and useful improvements in a METHOD AND APPARATUS FOR STACKING SEMICONDUCTOR CHIPS for which I have executed an application for Letters Patent in the United States, on even date herewith;

AND WHEREAS, Simple Technology Incorporated, a California Corporation, with its principal place of business at 3001 Daimler Street, Santa Ana, California 92705, desires to acquire the entire right, title, and interest in and to the said improvements and the said Application:

NOW, THEREFORE, in consideration of the sum of One Dollar ($1.00) to me in hand paid, and other good and valuable consideration, the receipt of which is hereby acknowledged, I, the said inventor, do hereby acknowledge that I have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto the said Simple Technology Incorporated, its successors, legal representatives and assigns, the entire right, title, and interest throughout the world in, to and under the said improvements, and the said application and all divisions, renewals and continuations thereof, and all Letters Patent of the United States which may be granted thereon and all reissues and extensions thereof, and all rights of priority under International Conventions and applications for Letters Patent which may hereafter be filed for said improvements in any country or countries foreign to the United States, and all Letters Patent which may be granted for said improvements in any country or countries foreign to the United States and all extensions, renewals and reissues thereof; and I hereby authorize and request the Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said improvements to the said Simple Technology Incorporated, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND I HEREBY covenant and agree that I will communicate to the said Simple Technology Incorporated, its successors, legal representatives and assigns, any facts known to me respecting said improvements, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing and reissue applications, make all rightful oaths and generally do everything possible to aid the said Simple Technology Incorporated, its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said improvements in all countries.

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 20 day of March 1995

[signature]
Mark Moshayedi

STATE OF

COUNTY OF } ss.

On March 20, 1995, before me, Mark Moshayedi, personally appeared Mark Moshayedi personally known to me (or proved to me on the basis of satisfactory evidence) to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

[SEAL]

Vicki L. Morrison
Signature

VICKI L. MORRISON
COMM. # 1040408
Notary Public — California
ORANGE COUNTY
My Comm. Expires SEP 30, 1998

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